08/24/00 JC905 U.S. PTO

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jc862 U.S. PTO 09/648403 08/24/00

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August 24, 2000

Attorney Docket No.: 08305/076001/99-29

Box Patent Application
Commissioner for Patents
Washington, DC 20231

Presented for filing is a new patent application claiming priority from a provisional patent application of:

Applicant: RICHARD H. TSAI

Title: P-TYPE RESET/READOUT CIRCUITRY WITH N-TYPE PHOTODIODE FOR RADIATION HARD APS

Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	Pages
Specification	11
Claims	6
Abstract	1
Declaration	2
Drawing(s)	8

Enclosures:
- Assignment cover sheet and an assignment, 2 pages, and a separate $40 fee.
- Small entity statement. This application is entitled to small entity status.
- Postcard.

Under 35 USC §119(e)(1), this application claims the benefit of prior U.S. provisional application 60/151,219, filed August 26, 1999.

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No EL584780267US

I hereby certify under 37 CFR §1.10 that this correspondence is being deposited with the United States Postal Service as Express Mail Post Office to Addressee with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

August 24, 2000
Date of Deposit

Derek Norwood
Signature

Derek Norwood
Typed or Printed Name of Person Signing Certificate

18 total claims, 3 independent.

Basic filing fee	$345
Total claims in excess of 20 times $9	$0
Independent claims in excess of 3 times $39	$0
Fee for multiple dependent claims	$0
Total filing fee:	$345

A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

If this application is found to be incomplete, or if a telephone conference would otherwise be helpful, please call the undersigned at (858) 678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

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4350 La Jolla Village Drive, Suite 500
San Diego, CA 92122

Respectfully submitted,

Reg No 42791

for Scott C. Harris
Reg. No. 32,030
Enclosures
SCH/nsg
10050200.doc

ATTORNEY DOCKET NO. 08305/076001/99-29

Applicant or Patentee: Richard H. Tsai
Serial or Patent No.:
Filed or Issued:
For: P-TYPE RESET/READOUT CIRCUITRY WITH N-TYPE PHOTODIODE FOR RADIATION HARD APS

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1.27(c)) — SMALL BUSINESS CONCERN

I hereby declare that I am

[] the owner of the small business concern identified below:
[X] an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Small Business Concern: PHOTOBIT CORPORATION
Address of Small Business Concern: 135 North Los Robles Avenue, 7th Floor
Pasadena, California 91101

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.802, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled P-TYPE RESET/READOUT CIRCUITRY WITH N-TYPE PHOTODIODE FOR RADIATION HARD APS by inventor(s) RICHARD H. TSAI described in:

[x] the specification filed herewith.
[]application serial no. _, filed _.
[] patent no. _, issued _.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e). *NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Full Name:
Address:

[] INDIVIDUAL [] SMALL BUSINESS CONCERN [] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status when any new rule 53 application is filed or prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent on which this verified statement is directed.

Name:	Angela L. McNamee
Title:	Secretary
Address:	135 North Los Robles Avenue, 7th Floor Pasadena, California 91101

Signature: Angela L. McNamee **Date:** 8/23/00

Attorney's Docket No.: 08305/076001 / 99-29

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: P-TYPE RESET/READOUT CIRCUITRY WITH N-TYPE PHOTODIODE FOR RADIATION HARD APS

APPLICANT: RICHARD H. TSAI

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EL584780267US

I hereby certify under 37 CFR §1.10 that this correspondence is being deposited with the United States Postal Service as Express Mail Post Office to Addressee with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

August 24, 2000
Date of Deposit

Signature

Derek Norwood
Typed or Printed Name of Person Signing Certificate

P-TYPE RESET/READOUT CIRCUITRY WITH N-TYPE PHOTODIODE FOR RADIATION HARD APS

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of the priority of U.S. Provisional Application No. 60/151,219, filed on August 26, 1999, and entitled P-Type Reset/Readout Circuitry for Radiation Hard APS.

BACKGROUND

The present disclosure generally relates to solid-state image sensors, and more specifically, to radiation hard active pixel sensors.

Charge coupled devices (CCD) have been used to process electronic image data. However, recent trend toward lower power consumption and greater system integration have spurred efforts to utilize existing sub-micron CMOS technology for electronic imaging applications.

Active pixel sensors (APS) are solid-state imagers where each pixel contains a photo-sensor, a photon to voltage converter, and a reset transistor. The APS detects image signals through a transistor switching rather than charge coupling. However, solid-state imagers may require a

protective enclosure in order to operate under radiation or space environment.

SUMMARY

In recognition of the above-described difficulties, the inventor recognized the need for providing a compact, radiation-hard active pixel sensor. Thus, the present disclosure discloses a pixel sensor that provides image sensing under radiation or space environment.

The pixel sensor includes a readout circuit and a first reset circuit. The readout circuit converts optical image signals to electronic signals, and includes p-type transistors and an n-type photosensitive element. The first reset circuit is configured to provide a reset level for a pixel output, and also includes p-type transistors. The use of p-type transistors and n-type photosensitive element provides radiation hardness without any radiation protective enclosure.

The present disclosure further includes a CMOS image sensor system, which includes an array of active pixel sensors, a control circuit, and a column readout circuit. Each pixel sensor of the array includes a pixel readout circuit and a first reset circuit. The pixel readout circuit converts optical image signals to electronic

signals, and includes p-type transistors and an n-type photosensitive element. The first reset circuit is configured to provide a reset level for a pixel output, and also includes p-type transistors. The control circuit provides timing and control signals to enable read out of data stored in the array of active pixel sensors. The column readout circuit receives and processes the data stored in the array of active pixel sensors.

BRIEF DESCRIPTION OF THE DRAWINGS

Different aspects of the disclosure will be described in reference to the accompanying drawings wherein:

FIG. 1 illustrates a conventional active pixel sensor and its associated readout circuitry;

FIG. 2 illustrates an embodiment of the present system configured to provide compact, radiation-hard active pixel sensor;

FIG. 3 shows a cross-section view of the pixel sensor;

FIG. 4 shows a simulation result with an active pixel sensor design;

FIG. 5 shows one implementation of a layout design using p-channel transistors and a square or a rectangular n-type photodiode;

FIG. 6 shows one implementation of a layout design using p-channel transistors and a circular photodiode;

FIG. 7 shows a pixel array having a mixture of p-channel transistors and an n-type photodiode;

FIG. 8A illustrates one embodiment of a typical size of a pixel sensor in accordance with the present system;

FIGS. 8B and 8C show minimum sizes of conventional pixel sensors, one having a square photodiode and another having a rectangular photodiode; and

FIG. 9 shows an embodiment of a CMOS image sensor system having pixels with n-type photodiodes and p-type transistors.

DETAILED DESCRIPTION

A conventional active pixel sensor and its associated readout circuitry are illustrated in FIG. 1. Each pixel 100 of the active pixel sensor may include a photosensitive element 102 buffered by a source-follower transistor 104 and a row selection switch, which can be implemented by a transistor 106. A signal "ROW" is applied to the gate of the row selection transistor 106 to enable a particular row of pixels. In some embodiments, the element 102 includes a photogate with a floating diffusion output separated by a transfer gate. In other embodiments, the photosensitive

element 102 includes a photodiode. Each pixel 100 also includes a reset switch that can be implemented as a transistor 108 controlled by a signal "RST" applied to its gate.

FIG. 1 further includes a column readout circuit 110 and an output stage 112. The column readout circuit 110 may include sample and hold circuits to sample both the reset and signal levels to reduce reset noise associated with the pixel as well as noise associated with the source-follower transistor 104. Multiple column readout circuits 110 are coupled to the output stage 112, which may include switched integrators. The output of the output stage 112 may be coupled to a source-follower transistor 114 and a load transistor 116. The illustrated conventional design of the active pixel sensor is often implemented with n-channel MOSFET transistors and a p-type photodiode as a photosensitive element 102. However, the above-described active pixel sensor design often requires a protective enclosure to operate under radiation or space environment.

The inventor recognized that p-channel MOSFET transistors provide significantly better protection against radiation than n-channel MOSFET transistors. A p-channel MOSFET transistor design also uses smaller silicon area. Further, a need for a protective enclosure may not be necessary with p-channel transistor design. However,

traditional p-type photodiodes often suffer from low quantum efficiency. The quantum efficiency provides a measure of conversion efficiency between photons picked up by a photosensitive element and a number of electrons converted from the photons. Further, possible latch-up problems, when reset level exceeds V_{DD} due to the charge injection of a switch, caused the prior designs to prefer n-channel transistors.

FIG. 2 illustrates an embodiment of the present system 200 configured to provide a compact, radiation-hard active pixel sensor. The system also produces a large output signal range that may be important for individual pixel reset application. In the illustrated embodiment, the active pixel sensor and its associated readout circuitry are implemented with p-channel transistors and an n-type photodiode as a photosensitive element 204. In one embodiment, the transistors are MOSFET transistors.

The p-channel MOSFET transistor design may provide radiation hardness without the need for a protective enclosure. In addition, the n-type photodiode provides better quantum efficiency than p-type photodiodes. Further, as illustrated in FIG. 3, the n-type photodiode configuration allows formation of p+ guard rings connected to the ground around the n-type photodiode. The grounded

guard rings may substantially reduce leakage current and prevent any latch-ups.

In the illustrated embodiment of FIG. 2, each pixel 202 of the active pixel sensor 200 may include an n-type photo-sensitive element 204 buffered by a p-channel MOSFET source-follower transistor 206 and a row selection switch which can be implemented by a p-channel MOSFET transistor 208. A signal "ROW" is applied to the gate of the row selection transistor 208 to enable a particular row of pixels. Each pixel 202 also includes a reset switch that can be implemented as a p-channel MOSFET transistor 210 controlled by a signal "RST" applied to its gate. An optional p-channel reset transistor 212 is provided for individual pixel reset application. This reset transistor 212 may allow a pixel-by-pixel reset operation instead of the row-by-row operation.

When R_{RST} is at logic low and C_{RST} at logic high, the reset switch 210 is turned off. However, the n-type well 306 (see FIG. 3) connected to V_{DD} allows the leakage current of a small photodiode (drain of the reset transistor) to charge the node 214 higher while the leakage current of an n-type reset transistor discharges the node 214 lower as the n-type photodiode. Thus, the p-channel transistors provide smaller leakage current than the n-channel transistors.

However, when R_{RST} is at logic low and C_{RST} at logic low, the reset switch 210 may be turned on by a p-channel threshold voltage (V_{thp}) at the gate of the reset switch 210. The above-described configuration resets the node 214 to V_{RST}, which is equal to V_{DD} minus a small voltage of about 0.7 volts (V_{thp}). This reset voltage (V_{RST}) further prevents any latch-up problems caused by a reset level exceeding V_{DD} due to the charge injection of the reset switch.

The reset voltage (V_{RST}) needs to stay below the supply voltage (V_{DD}) to keep the p-channel source follower transistor 206 in the linear region. By keeping the source follower 206 in the linear region, the active pixel sensor has hard reset levels such as small fixed pattern noise and uniform reset levels.

The p-channel transistor design of the active pixel sensor 200 also includes p-channel load transistors 216, 218 and a p-channel output source-follower 220.

Referring to FIG. 3, the n-type photodiode 300 is guarded by a pair of p+ guard rings 302 connected to the ground. The photodiode 300 and the guard rings 302 are provided over a p-type substrate 304. N-type wells 306 on either side are connected to V_{DD}. The wells 306 are configured to prevent crosstalk between pixels.

A simulation result with an active pixel sensor design as described above is shown in FIG. 4. The result shows

that when a row is selected, the output follows the voltage level of PIX node 214. When C_{RST} (along with R_{RST}) is set to logic low, PIX node 214 is reset to V_{RST}. Thus, the active pixel sensor of the present system provides large output swing and hard reset level. As a result, the dynamic range of the sensor increases.

FIGS. 5 through 7 illustrate different layout implementations of the active pixel sensor using the design described above. FIG. 5 shows one implementation of a layout design using p-channel transistors and a square or a rectangular n-type photodiode. FIG. 6 shows one implementation of a layout design using p-channel transistors and a circular photodiode. FIG. 7 shows a pixel array having a mixture of above-described pixel designs. This pixel array may be used in an active pixel sensor design to provide image sensing under radiation environment.

FIGS. 8A to 8C show comparison of areal density between the p-channel transistor/ n-type photodiode design and conventional n-channel transistor designs.

FIG. 8A illustrates one embodiment of a typical size of a pixel sensor in accordance with the present system. The pixel sensor has an n-channel square photodiode. The minimum size of this pixel sensor is measured to be approximately (14 μm)^2.

FIGS. 8B and 8C show minimum sizes of conventional pixel sensors, one having a square photodiode and another having a rectangular photodiode. The rectangular photodiode design requires minimum size of approximately $(21\ \mu m)^2$ while the square photodiode requires minimum size of approximately $(28\ \mu m)^2$. Thus, it is shown that pixel sensor design of the present system requires less than half the size of the conventional design. Further, the conventional design would also require a bulky enclosure to protect the pixel array from the radiation.

FIG. 9 shows an embodiment of a CMOS image sensor system 900. The system includes an array of active pixel sensors 902 and a controller 904. Each active pixel sensor may be implemented with p-channel MOSFET transistors and an n-type photodiode. The controller 904 provides timing and control signals to enable read out of signals stored in the pixels.

The image array 902 data is read out a row at a time using column-parallel readout architecture, as illustrated by a column readout circuit 110 in FIG. 1. The controller 904 selects a particular row of pixels in the array 902 by controlling the operation of the vertical addressing circuit 906 and row drivers 908. Charge signals stored in the selected row of pixels are provided to a readout circuit

910. The pixels read from each of the columns can be read out sequentially using a horizontal addressing circuit 914. The output of the readout circuit 910 is directed to an output stage buffer 912. The output stage buffer 912 includes a p-type source-follower MOSFET transistor similar to the source-follower 220, and a p-type load transistor 218 as shown in FIG. 2.

While specific embodiments of the invention have been illustrated and described, other embodiments and variations are possible. For example, although the transistors used in the pixel sensors have been described in terms of MOSFET transistors, other types of transistors, such as JFET or bipolar transistors, may be used in the pixel sensors.

All these are intended to be encompassed by the following claims.

What is claimed is:

1. A pixel sensor for providing image sensing under radiation or space environment, comprising:

a readout circuit operating to convert optical image signals to electronic signals, where said readout circuit includes p-type transistors and an n-type photosensitive element; and

a first reset circuit configured to provide a reset level for a pixel output, where said first reset circuit includes at least one p-type transistor,

where said readout circuit and said first reset circuit having said p-type transistors, and said n-type photosensitive element, provide radiation hardness without any radiation protective enclosure.

2. The pixel sensor of claim 1, wherein said p-type transistors are MOSFET p-type transistors.

3. The pixel sensor of claim 1, wherein said n-type photosensitive element is an n-type photodiode.

4. The pixel sensor of claim 3, wherein said n-type photodiode is formed in a square layout design.

5. The pixel sensor of claim 3, wherein said n-type photodiode is formed in a circular layout design.

6. The pixel sensor of claim 1, further comprising:

a p-type substrate on which said n-type photosensitive element is formed.

7. The pixel sensor of claim 6, further comprising:

a pair of p+ type guard rings formed on said p-type substrate, each of said pair of guard rings formed on either side of said n-type photosensitive element, said pair of guard rings connected to a ground voltage, and operating to substantially reduce a leakage current from said n-type photosensitive element.

8. The pixel sensor of claim 6, further comprising:

an n-type well provided adjacent to said p-type substrate, said n-type well connected to a supply voltage, and operating to prevent crosstalk between pixels.

9. The pixel sensor of claim 1, further comprising:

a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

10. A radiation-hard CMOS image sensing device, comprising:

a p-type substrate;

an n-type photodiode formed on said p-type substrate, where said n-type photodiode operates to convert an optical signal to an electrical signal;

a first reset circuit configured to provide a reset value for said electrical signal, said first reset circuit including a p-type MOSFET transistor; and

a readout circuit operating to buffer said electrical signal, said readout circuit including a p-type MOSFET transistor.

11. The device of claim 10, further comprising:

a pair of p+ type guard rings formed on said p-type substrate, each of said pair of guard rings formed on either side of said n-type photodiode, said pair of guard rings connected to a ground voltage, and operating to substantially reduce a leakage current from said n-type photodiode.

12. The device of claim 11, further comprising: an n-type well provided adjacent to said p-type substrate, said n-type well connected to a supply voltage, and operating to prevent crosstalk between pixels in the CMOS image sensing device.

13. The device of claim 10, further comprising: a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

14. A CMOS image sensor system, comprising:

an array of active pixel sensors, each pixel sensor of said array including:

a pixel readout circuit operating to convert optical image signals to electronic signals, where said pixel readout circuit includes p-type transistors and an n-type photosensitive element, and

a first reset circuit configured to provide a reset level for a pixel output, where said first reset circuit includes p-type transistors,

where said pixel readout circuit and said first reset circuit having said p-type transistors and said n-type photosensitive element provide radiation hardness without any radiation protective enclosure;

a control circuit configured to provide timing and control signals to enable read out of data stored in said array of active pixel sensors; and

a column readout circuit operating to receive and process said data stored in said array of active pixel sensors.

15. The CMOS image sensor of claim 14, further comprising:

a p-type substrate on which said n-type photosensitive element is formed.

16. The CMOS image sensor of claim 15, further comprising:

a pair of p+ type guard rings formed on said p-type substrate, each of said pair of guard rings formed on either side of said n-type photosensitive element, said pair of guard rings connected to a ground voltage, and operating to substantially reduce a leakage current from said n-type photosensitive element.

17. The CMOS image sensor of claim 15, further comprising:

an n-type well provided adjacent to said p-type substrate, said n-type well connected to a supply voltage, and operating to prevent crosstalk between pixels.

18. The CMOS image sensor of claim 14, further comprising:

a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

ABSTRACT

A pixel sensor that provides image sensing under radiation or space environment is disclosed. The pixel sensor includes a readout circuit and a first reset circuit. The readout circuit converts optical image signals to electronic signals, and includes p-type transistors and an n-type photosensitive element. The first reset circuit is configured to provide a reset level for a pixel output, and also includes p-type transistors. The use of p-type transistors and n-type photosensitive element provides radiation hardness without any radiation protective enclosure.

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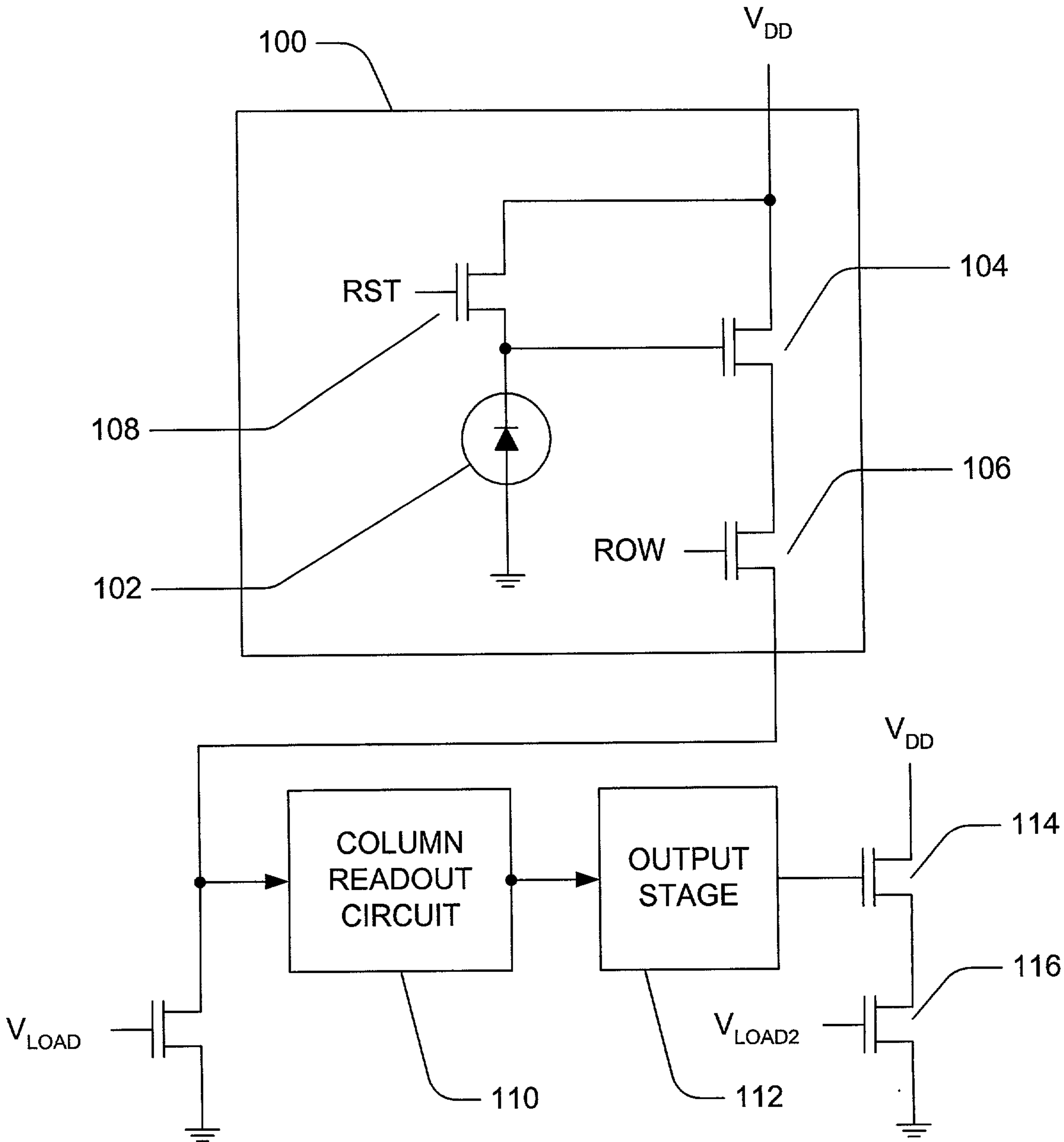


FIG. 1
(PRIOR ART)

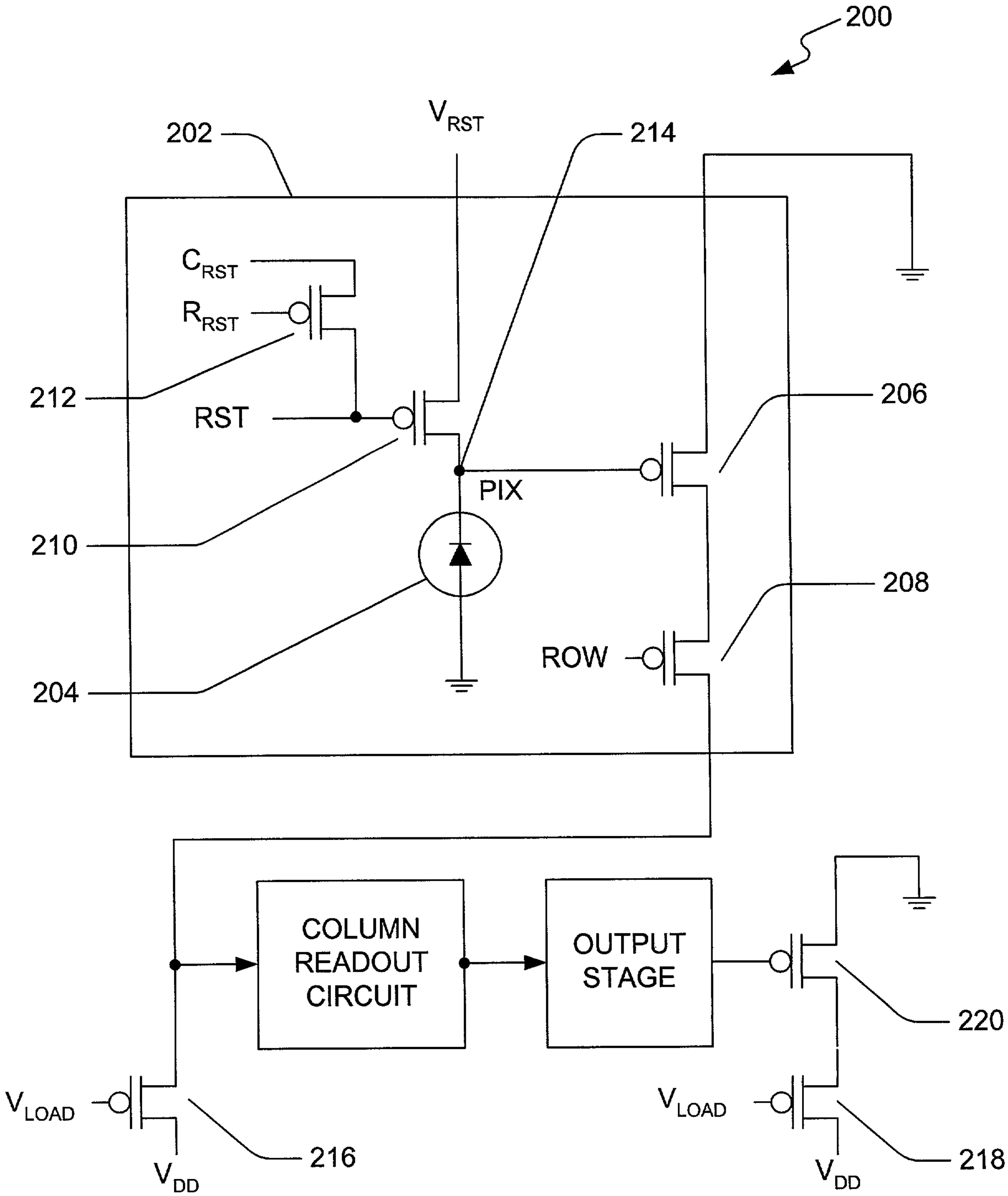

200
202
V_{RST}
214
C_{RST}
R_{RST}
212
RST
206
PIX
210
208
ROW
204
COLUMN READOUT CIRCUIT
OUTPUT STAGE
220
V_{LOAD}
216
V_{DD}
V_{LOAD}
218
V_{DD}

FIG. 2

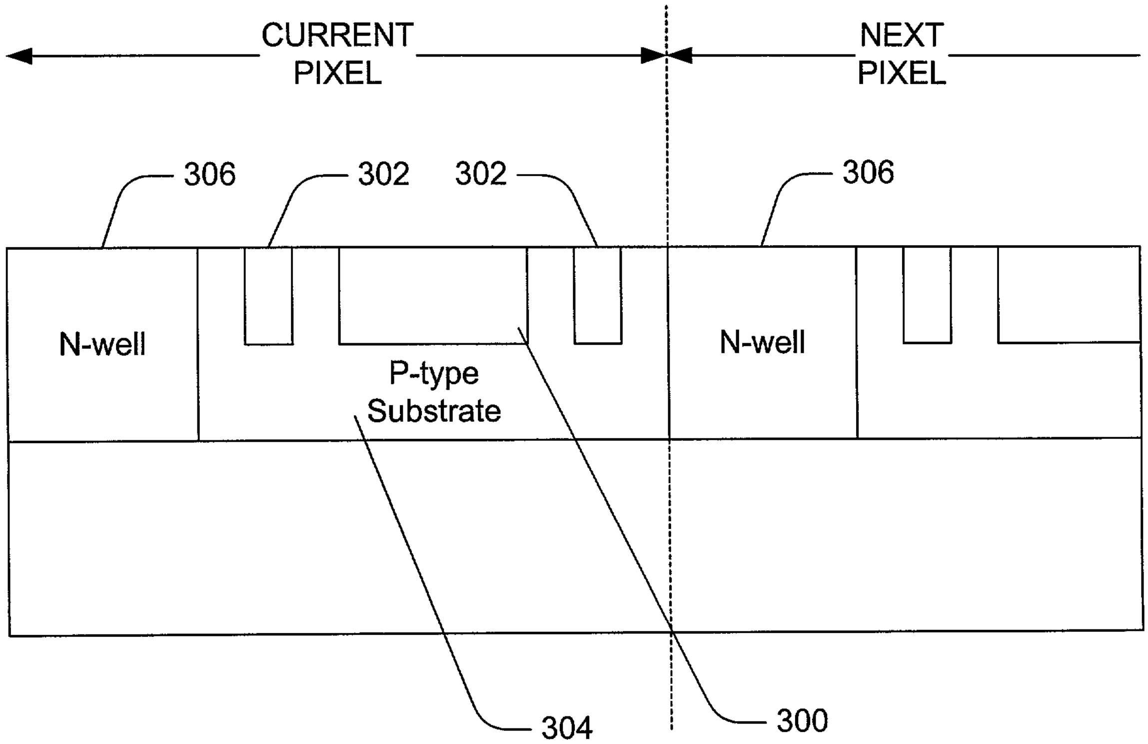
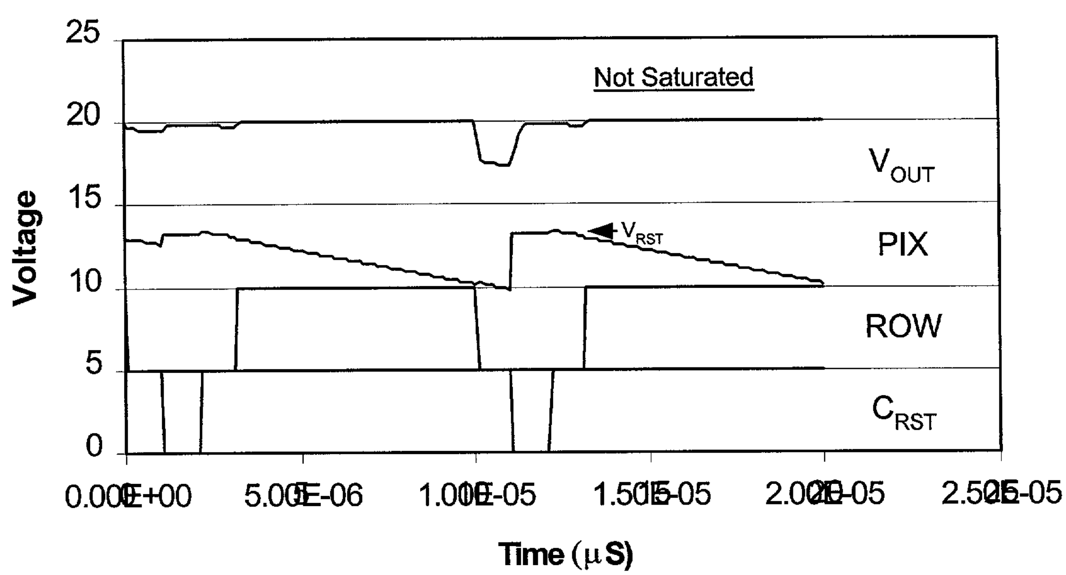

CURRENT
PIXEL
NEXT
PIXEL
306
302
302
306
N-well
P-type
Substrate
N-well
304
300

FIG. 3


25
20
15
10
5
0
Voltage
Not Saturated
V_{OUT}
PIX
V_{RST}
ROW
C_{RST}
0.00E+00
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1.00E-05
1.50E-05
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2.50E-05
Time (μS)

FIG. 4

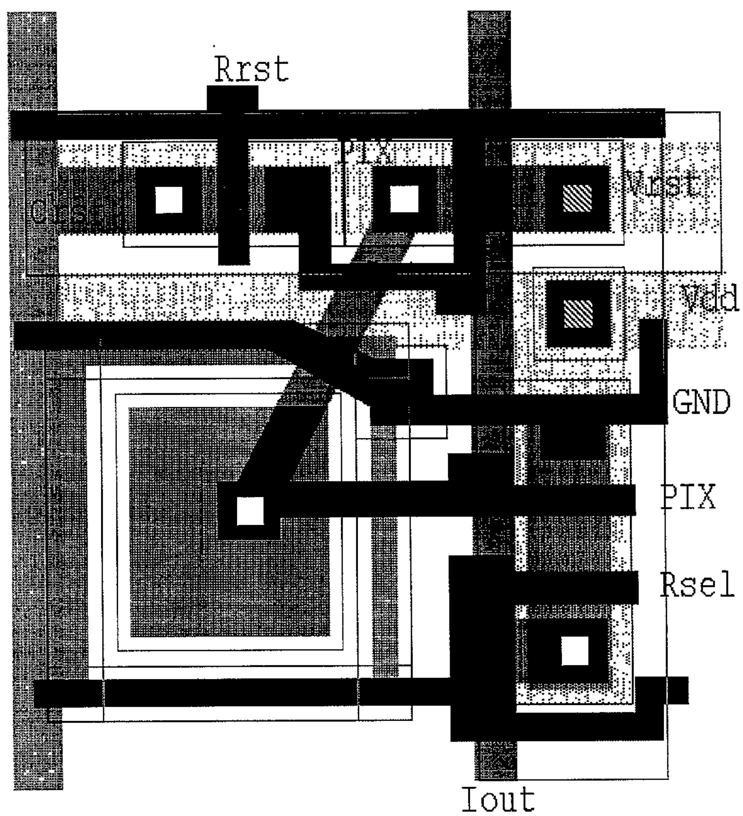

FIG. 5

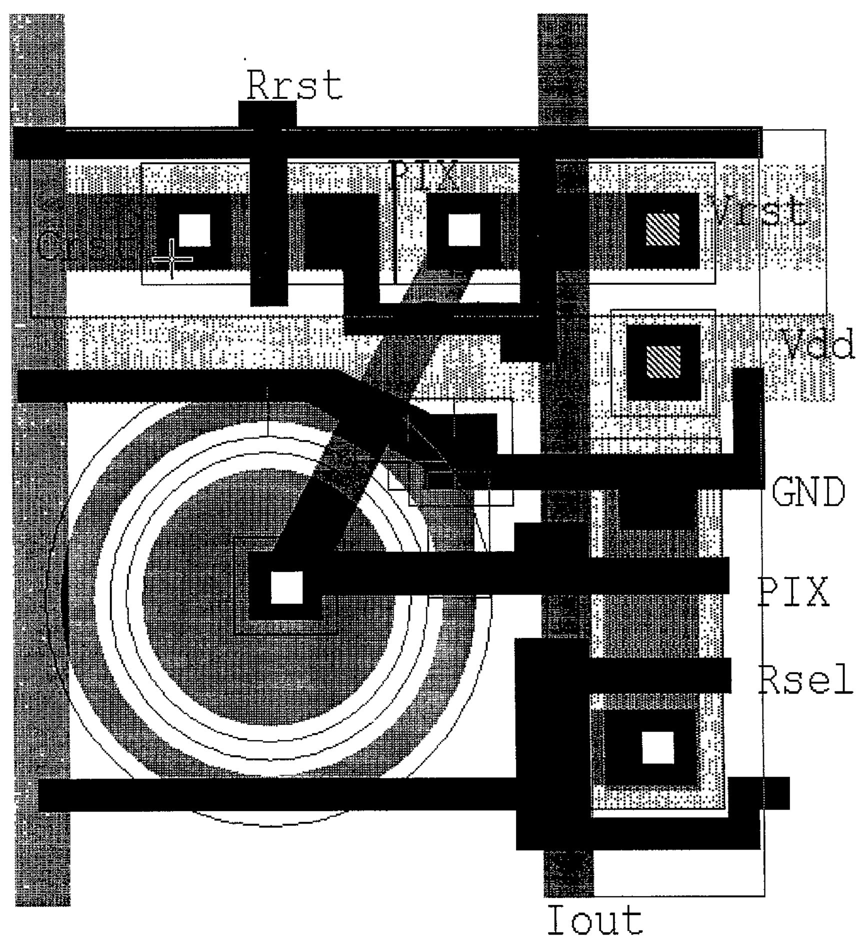

FIG. 6

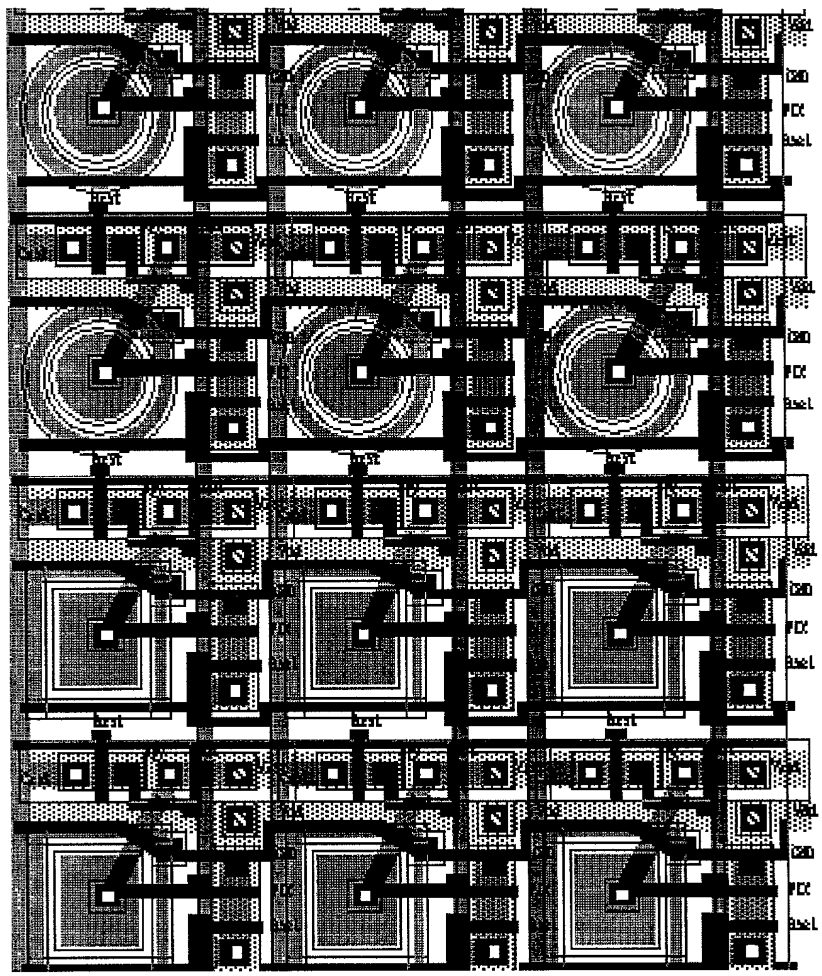

FIG. 7

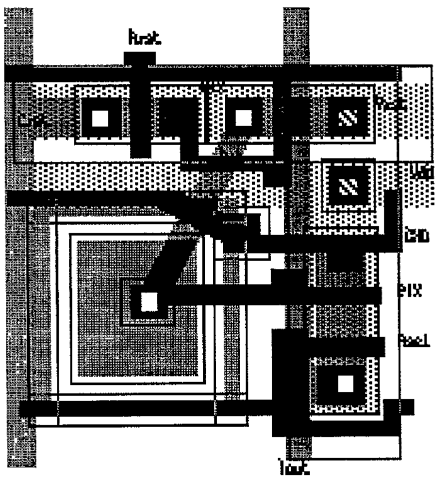

FIG. 8A

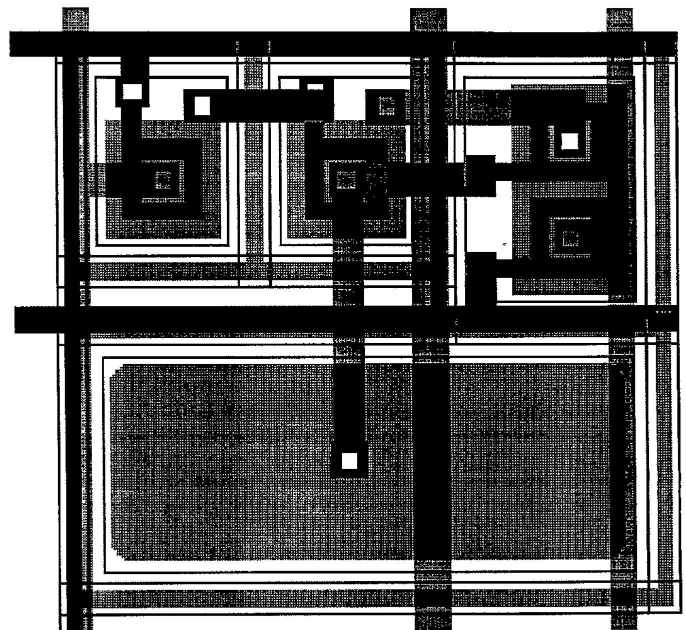

FIG. 8B

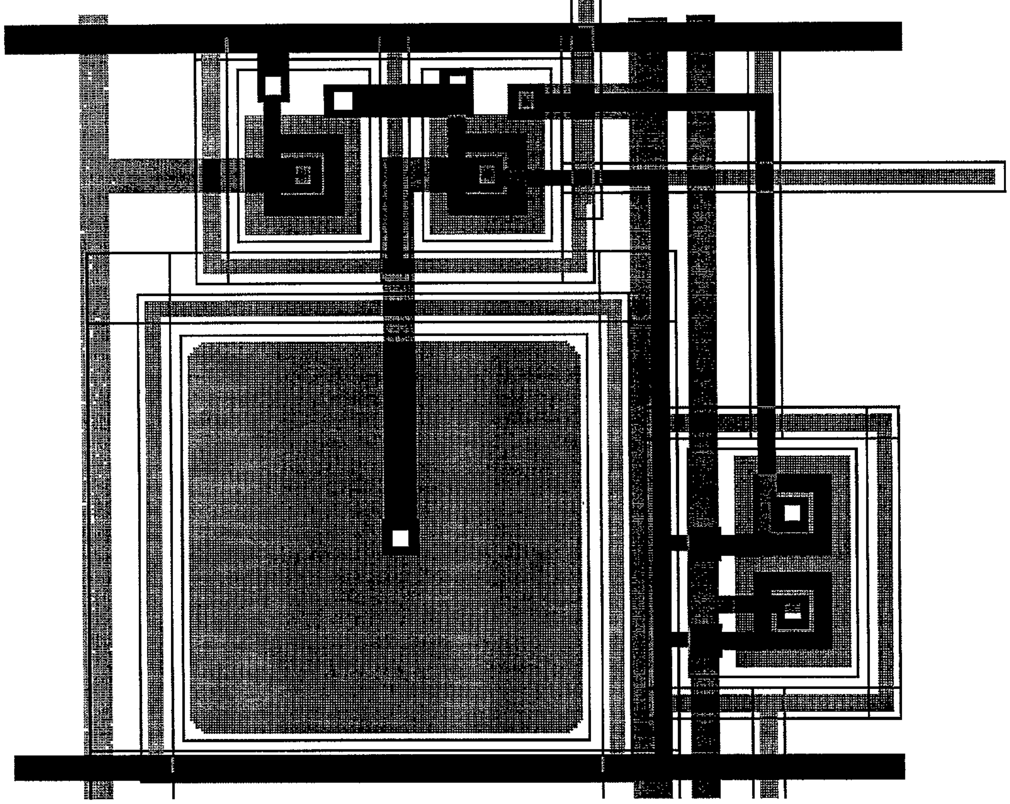

FIG. 8C

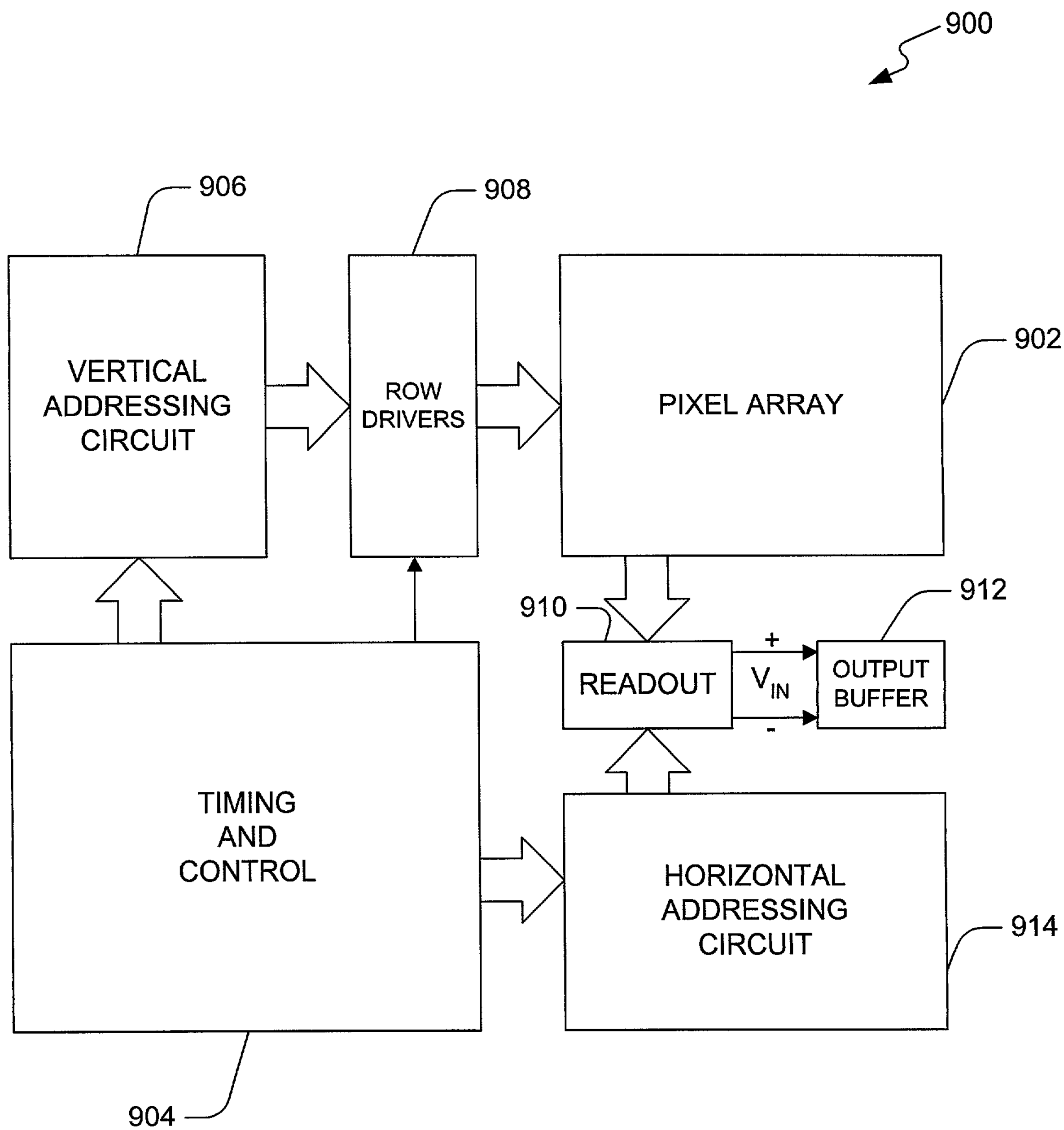
900
906
908
VERTICAL ADDRESSING CIRCUIT
ROW DRIVERS
PIXEL ARRAY
902
910
912
READOUT
+
V_{IN}
-
OUTPUT BUFFER
TIMING AND CONTROL
HORIZONTAL ADDRESSING CIRCUIT
914
904

FIG. 9

Attorney Docket No. 08305/076001/99-29

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled P-TYPE RESET/READOUT CIRCUITRY WITH N-TYPE PHOTODIODE FOR RADIATION HARD APS, the specification of which:

[X] is attached hereto.
[] was filed on ____ as Application Serial No. ____ and was amended on ______________.
[] was described and claimed in PCT International Application No. ______________ filed on ______________ and as amended under PCT Article 19 on ______________.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit under Title 35, United States Code, §119(e)(1) of any United States provisional application(s) listed below:

U.S. Serial No.	Filing Date	Status
60/151,219	August 26, 1999	Pending

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information I know to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

U.S. Serial No.	Filing Date	Status

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Country	Application No.	Filing Date	Priority Claimed

Attorney Docket No. 08305/076001/99-29

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